Refine Search

Search Results -

Terms	Documents
L10 same memory same test	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L16

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, February 02, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L16	L10 same memory same test	2	L16
L15	L14 same load	7	L15
L14	L10 same cam	123	L14
L13	L10 same l4	3	L13
L12	L11 same l4	0	L12
L11	L10 same l2	8	L11
L10	dischargeline or (discharge adj1 line)	12178	L10
L9	L8 same load	10	L9
L8	L1 same test	114	L8
L7	L1 same l4	5	L7
L6	L2 same l4	3	L6
L5	L4 same l3	0	L5
L4	test adj1 circuit	10245	L4
L3	L2 same l1	0	L3

L2	(variable adj1 load) or (switchable adj1 load)	3247	L2
L1	matchline or (match adj1 line)	2026	L1

END OF SEARCH HISTORY

L7: Entry 1 of 5 File: USPT Feb 24, 2004

DOCUMENT-IDENTIFIER: US 6697277 B2
TITLE: Content addressable memory (CAM) having a match line circuit with selectively adjustable pull-up impedances

Detailed Description Text (16):
Accordingly, FIG. 5 illustrates a reference circuit 500 which features devices substantially similar to those included within circuit 300, and which are preferably formed upon the same chip as circuit 300 and the CAM array. However, in contrast to a plurality of circuits 300 associated with the CAM array cells, there need only be a single reference circuit 500. In effect, reference circuit 500 is used as a "dummy" or test circuit which is self-adjusting so as to determine a desired impedance strength for the pull-up devices included in the actual operating match line circuits 300.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 2 of 5 File: USPT Sep 9, 2003

DOCUMENT-IDENTIFIER: US 6618279 B2
TITLE: Method and apparatus for adjusting control circuit pull-up margin for content addressable memory (CAM)

Detailed Description Text (16):
Accordingly, FIG. 5 illustrates a reference circuit 500 which features devices substantially similar to those included within circuit 300, and which are preferably formed upon the same chip as circuit 300 and the CAM array. However, in contrast to a plurality of circuits 300 associated with the CAM array cells, there need only be a single reference circuit 500. In effect, reference circuit 500 is used as a "dummy" or test circuit which is self-adjusting so as to determine a desired impedance strength for the pull-up devices included in the actual operating match line circuits 300.

Previous Doc Next Doc Go to Doc#

L9: Entry 9 of 10 File: USPT Jul 14, 1987

DOCUMENT-IDENTIFIER: US 4680760 A
TITLE: Accelerated test apparatus and support logic for a content addressable memory

Abstract Text (1):
Accelerated test circuitry and support logic to test a content addressable memory (CAM). In a CAM array of n entries of m bits per entry, the testing of each word lind, each memory element, each exclusive OR (XOR) comparator and each match line may be thoroughly and quickly tested by means of the parallelism inherent in a CAM array and by the addition of a bulk load mechanism to enable all of the word lines simultaneously. The further addition of an ALLHIT indicator to assess all of the match lines in a single operation also reduces the number of operations and simplifies the test algorithm. The ALLHIT indicator may be an AND gate or a scan path.

Detailed Description Text (21):
The remaining test complexity is due to the writing and comparing of unique data in every entry 12 (steps 1 through 5 of the basic algorithm). The only reason this is necessary is due to the fact that observability of the CAM array 10 is funneled through HIT/MISS* 30 which is the output of OR gate 32, forcing the observer to enable only one match line 18 at a time. An ALLHIT indicator is provided which is composed of two parts, line 38, which is an output from functional block 40 having as inputs all n match lines 18. The ALLHIT indicator 38 and 40 can collapse the n term out of the complexity factor. Functional block 40 may be an AND gate, as will be assumed in the following discussion, or may be a scan path, as will be discussed later. Ideally, ALLHIT 38 is made an additional primary output. With the ALLHIT indicator 38 and the bulk load feature 42, the algorithm simplifies to the following:

Detailed Description Text (31):
It is noted that the ALLHIT feature 38 and its AND gate 40, as well as HIT/MISS* 30 and its OR gate 32 each require n+1 tests and are not covered in the new algorithm above. It is submitted that this new algorithm will catch all single stuck-at-faults in the array 10. Again, regardless of the design of the entry selection circuitry 34, it is reasonable that the circuitry 34's test would include at least n CAM entry 12 loads. These loads will each cause a hit and can catch all the HIT/MISS* 30 input (match lines 18) SA0 faults.

Detailed Description Text (34):
An alternate form of the ALLHIT strategy is possible. Instead of using an AND gate 40 for the ALLHIT output 38, a scan path (i.e. a shift register) that captures the state of the match lines 18 could be added. ALLHIT 38 would then shift out the test result information in a serial bit stream. This would mean that the single operations in steps B, D and G of the new algorithm would now be n scan clocks (not to be confused with the system clocks). The complexity is 2m+3 operations plus 3n scan clocks, assuming that a scan clock is somewhat less of an operation than either a compare for CAM 10 contents or a CAM 10 load. Scan paths, if they are a loop, are easily testable. Also, some types of entry addressing circuitry 34 might lend themselves to inclusion of an ALLHIT scan path test mode function with little additional overhead. Whatever the absolute overhead, its percentage compared to

main circuitry is proportional to n/m to first order.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L9: Entry 2 of 10 File: USPT Jul 19, 2005

DOCUMENT-IDENTIFIER: US 6920525 B2
TITLE: Method and apparatus of local word-line redundancy in CAM

Detailed Description Text (4):
Exemplary details of the match-line circuitry 2 of the memory array in FIG. 1 are shown in FIG. 3. Since match-lines are coincident with word-lines, there is no need for redundant match-lines. Therefore, the match-line outputs must be steered as well, in order to account for word-line shifting or steering. Without match-line steering, match-line n would not be coincident with word-line n when redundancy is implemented. Redundancy MUXs 31 are again used to perform steering function. As previously stated, these MUXs 31 (and 71 in FIG. 7) receive their select input from the redundancy latches. The MUXs feed match-line latches 32 (and 52 and 72 in FIGS. 5 and 7, respectively) which in turn feed the BIST compare structure 34. The BIST compare latches 33 (and 53 and 73 in FIGS. 5 and 7, respectively) are used to load test `expect match/mismatch` data for comparing against match-line test results. The BIST compare latches 33 feed XNOR circuitry 34 which compares the match-line outputs to the test `expect match/mismatch` data. This logic provides a means for identifying failing match-lines. These results are captured in failing match-line "sticky" latches 35 (and 54 and 74 in FIGS. 5 and 7, respectively) which are used in conjunction with read word-line stored address data in the BIST logic design to determine if repair using redundancy is possible, and if so, what to replace. BIST testing details will be discussed later.

Detailed Description Text (10):
As illustrated in FIG. 9, a method of implementing word-line redundancy involves using BIST 91, 93 to test both read/write and match-line operations, record failing read addresses 92, compress the failing match-line values into failing match-line addresses 94, compare the failing read/write fail addresses with the match-line fail addresses 95, determine if repair with redundancy is possible 96 and, if so, use the failing read/write and/or failing match-line address data to blow fuses 98. The fuse data can then be accessed before functional operation, to load redundancy information into the redundancy latches for steering.

Previous Doc Next Doc Go to Doc#

L16: Entry 1 of 2 File: USPT Sep 10, 2002

DOCUMENT-IDENTIFIER: US 6449740 B1
TITLE: Conductive paths controllably coupling pad groups arranged along one edge to CPU and to EEPROM in test mode

Detailed Description Text (22):
The external tester supplies the address signal to the input/output port PORT4, and the address signal is transferred to the address port of the EEPROM 36. An internal sense amplifier flows current to the memory cells at the memory location, and checks the potential level on the current path to see whether or not the memory cells flow the current to a discharge line. If the test pattern has changed a selected memory cell to a high threshold, the selected memory cell does not offer any conductive channel, and no current flows. For this reason, the current path keeps the potential level high. On the other hand, if the test pattern has changed the selected memory cell to a low threshold, the selected memory cell offers a conductive channel between the current path and the discharge line, and discharges the current. This results in that the current path decays the potential level. Test bits of the test pattern are stored in the memory cells in the form of the threshold, and the sense amplifier discriminates the stored bits on the basis of the potential level on the current path. The sense amplifier produces output data signal indicative of the read-out test pattern, and the output data signal is supplied from the data port through the shared bus system 38, the set of signal lines 70, the input/output port PORT6 and the communication pads 40 to the external tester. The external tester compares the read-out test patter with the write-in test pattern to see whether or not the memory cells maintain the test pattern without inversion of a test bit. The above-described sequence is repeated for all the memory cells, and the external tester diagnoses the EEPROM 36 as either defective or non-defective.

Detailed Description Text (50):
The EEPROM connects the sense amplifier to the memory cells assigned the address through current paths, and the sense amplifier flows current through the current paths to the selected memory cells. The sense amplifier checks the potential levels on the current paths to see whether or not the selected memory cells discharge the current. If the memory cell discharges the current, the potential level on the associated current path becomes lower than the threshold. On the other hand, if the memory cell isolates the associated current path from a discharge line, the potential level exceeds the threshold. The sense amplifier determines the logic level of the test bits stored in the selected memory cells, and supplies an eight-bit data signal representative of read-out test patterns to the output data port.